CLAIMS

What is claimed is:

1. A method, comprising:

modeling an etch process used in semiconductor manufacturing to generate a dynamic process model; and

optimizing a process recipe for the etch process with the dynamic process model.

2. The method of claim 1, wherein the etch process is a cell formation process.

3. The method of claim 1, wherein the dynamic process model is a linear ARX model with input nonlinearities.

4. The method of claim 1 wherein the optimized process recipe improves cell sidewall profiles.

5. The method of claim 4, wherein the optimized process recipe incorporates a maximum allowable number of recipe steps as an explicit process constraint.

6. The method of claim 4, wherein the optimized process recipe incorporates a maximum allowable input value as an explicit process constraint.

7. The method of claim 4, wherein the optimized process recipe incorporates a minimum allowable input value as an explicit process constraint.

8. The method of claim 1, wherein modeling an etch process, comprises:

using a non-linear model structure;

paramaterizing the memoryless non-linear functions;

deriving a linear model from the non-linear model structure;

identifying a bias value for distinct input parameters and output parameters;

generating a dynamic spatial model of output parameters to relate input parameters in a time domain to output parameters in a spatial domain;

predicting output parameters when various input parameters are provided to the linear model; and

optimizing output parameters using the linear model.

9. The method of claim 8, wherein the dynamic spatial model is a deposition rate model;

10. The method of claim 8, wherein the input parameters include dopant gas flows including TriEthyl Borate, TriEthyl PhOsphate, and TetraEthyl OrthoSilicate; and plasma etch inputs including pressure, power, and gas flows.

11. The method of claim 8, wherein the output parameters include chemical vapor deposition outputs including Secondary Ion Mass Spectrometry dopant profiles before and after reflow, Fourier Transform Infrared Spectroscopy aggregate dopant profiles, plasma etch outputs, and wet clean outputs including electrical measurements, critical dimension measurements, Scanning Electron Microscopy cross-section sidewall profiles before and after wet etch in both X and Y directions.

12. The method of claim 1, further comprising manufacturing a semiconductor wafer have cell profile deviations of less than 100 angstroms.

13. The method of claim 8, wherein the non-linear model structure is an INARX model with memoryless non-linear functions to capture dynamic etch process behaviors.